WHAT IS CLAIMED IS:

1. An address generator that generates an address sequence directly to memory, comprising:

a control unit including a plurality of counters that count between predefined start and stop values and generates first, second and offset values;

an adder to combine first, second and offset values and generate an address value; and

a multiplexer to receive a first value, second value and address value and select an output value to a memory.

2. The address generator claimed in claim 1, wherein the plurality of counters comprise:

a first counter that indexes in a first direction in memory; and

a second counter that indexes in a second direction in memory.

3. The address generator claimed in claim 2, wherein the control unit further comprises:

first and second start registers that store start values for the first and second counters.

4. The address generator claimed in claim 3, wherein the control unit further comprises:

first and second stop registers that store the stop values for the first and second counters.

5. The address generator claimed in claim 4, wherein the control unit further comprises:

first and second length registers that store the length values for the first and second counters to take until they go back to the last starting value plus the slip.

6. The address generator claimed in claim 5, wherein the control unit further

comprises:

first and second step registers that store the step values for the first and second counters to count by.

7. The address generator claimed in claim 6, wherein the control unit further comprises:

first and second slip registers that store the slip values for the first and second counters to count by.

8. The address generator claimed in claim 7, wherein the control unit further comprises:

first and second slip after length mode registers to allow activation of the slip after length modes for first and second counters.

9. The address generator claimed in claim 8, wherein in the slip after length mode, the previous start value plus slip is used to calculate the new start value after the counter length has occurred.

10. The address generator claimed in claim 9, wherein the control unit further comprises:

first and second slip after stop mode registers to allow activation of the slip after stop modes for first and second counters.

11. The address generator claimed in claim 10, wherein in the slip after stop mode, the slip register is applied after the counter stop is reached.

12. The address generator claimed in claim 11, wherein the slip after stop mode is used for JPEG 2000 scanning.

13. The address generator claimed in claim 11, wherein the control unit further comprises:

first and second count after stop mode registers to allow activation of the count after stop mode.

14. The address generator claimed in claim 13, wherein in the count after stop mode, a first counter is used to trigger a second counter to count in response to a stop value being reached and after a length count has finished.

15. The address generator claimed in claim 14, wherein the control unit further comprises:

first and second count after length mode registers to allow activation of the count after length mode.

16. The address generator claimed in claim 15, wherein in the count after length mode, a first counter triggers a second counter in response to a length amount being counted.

17. The address generator claimed in claim 16, wherein the control unit further comprises:

an offset register that stores an offset value that is added to the first and second counter values to produce a physical address to memory.

18. The address generator claimed in claim 1, wherein the selected first value, second value or address value is applied to the memory as a source or destination address for memory load and stores.

19. The address generator claimed in claim 1, wherein the generator receives control from a processor s instruction that directly and indirectly indexed causes the selected first value, second value or address value to be applied to the memory as a source or destination address for memory load and stores.

20. A method for generating an address sequence to memory, comprising:

defining parameter values including start and stop values;

counting between predefined start and stop values;

generating first, second and offset values;

combining first, second and offset values and generating an address value;

selecting a first value, second value or address value; and

using the selected value to directly or indirectly access memory.

21. The method claimed in claim 20, wherein counting between predefined start and stop values further comprises:

indexing in a first direction in memory; and

indexing in a second direction in memory.

22. The method claimed in claim 21, wherein defining parameter values including start and stop values further comprises:

accessing X and Y start values.

23. The method claimed in claim 22, wherein defining parameter values including start and stop values the further comprises:

accessing X and Y stop values.

24. The method claimed in claim 23, wherein defining parameter values including start and stop values further comprises:

accessing first and second length values for first and second counters to take until they go back to the last starting value plus the slip.

25. The method claimed in claim 24, wherein defining parameter values including start and stop values further comprises:

accessing first and second step values for the first and second counters to count by.

26. The method claimed in claim 25, wherein defining parameter values including start and stop values further comprises:

accessing first and second slip values for the first and second counters to count by.

27. The method claimed in claim 20, wherein defining parameter values including start and stop values further comprises:

enabling first or second slip after length modes to allow activation of the slip after length modes for first or second counters.

28. The method claimed in claim 27, wherein enabling first or second slip after length modes to allow activation of the slip after length modes for first or second counters further comprises:

using a previous start value plus slip to calculate the new start value after the counter length has occurred.

29. The method claimed in claim 28, wherein defining parameter values including start and stop values further comprises:

enabling first or second slip after stop modes to allow activation of the slip after stop modes for first or second counters.

30. The method claimed in claim 29, wherein enabling first or second slip after stop modes to allow activation of the slip after stop modes for first or second counters further comprises:

applying the slip value after the counter stop is reached.

31. The method claimed in claim 30, further comprising:

enabling the slip after stop mode for JPEG 2000 scanning.

32. The method claimed in claim 30, wherein defining parameter values including start and stop values further comprises:

enabling first or second count after stop modes to allow activation of the count after stop mode.

33. The method claimed in claim 32, wherein enabling first or second count after stop modes to allow activation of the count after stop mode further comprises:

using a first counter to trigger a second counter to count in response to a stop value being reached and after a length count has finished.

34. The method claimed in claim 33, wherein defining parameter values including start and stop values further comprises:

enabling first or second count after length mode registers to allow activation of the count after length mode.

35. The method claimed in claim 34, wherein enabling first or second count after length mode registers to allow activation of the count after length mode further comprises:

using a first counter to trigger a second counter in response to a length amount being counted.

36. The method claimed in claim 35, wherein defining parameter values including start and stop values further comprises:

accessing an offset value that is added to the first and second counter values to produce a physical address to memory.

37. The method claimed in claim 20, further comprising:

applying the selected first value, second value or address value to the memory as a source or destination address for memory load and stores.

38. The method claimed in claim 20, further comprising:

receiving control from a processor s instruction that directly and indirectly indexed causes the selected first value, second value or address value to be applied to the memory as a source or destination address for memory load and stores.

39. A system, comprising:

a memory;

a control unit including a plurality of counters that count between predefined start and stop values and generates first, second and offset values;

an adder to combine first, second and offset values and generate an address value; and

a multiplexer to receive a first value, second value and address value and select an output value to the memory, the output value comprises an address sequence directly to the memory.

40. The system claimed in claim 39, wherein the plurality of counters comprise:

a first counter that indexes in a first direction in memory; and

a second counter that indexes in a second direction in memory.

41. The system claimed in claim 40, wherein the control unit further comprises:

first and second start registers that store start values for the first and second counters;

first and second stop registers that store the stop values for the first and second counters;

first and second length registers that store the length values for the first and second counters to take until they go back to the last starting value plus the slip;

first and second step registers that store the step values for the first and second counters to count by;

first and second slip registers that store the slip values for the first and second counters to count by; and

an offset register that stores an offset value that is added to the first and second counter values to produce a physical address to memory.

42. The address generator claimed in claim 41, wherein the control unit further comprises:

first and second slip after length mode registers to allow activation of the slip after length modes for first and second counters;

first and second slip after stop mode registers to allow activation of the slip after stop modes for first and second counters;

first and second count after stop mode registers to allow activation of the count after stop mode; and

first and second count after length mode registers to allow activation of the count after length mode.

43. The system claimed in claim 42, wherein the selected first value, second value or address value is applied to the memory as a source or destination address for memory load and stores.

44. The system claimed in claim 43, wherein the generator receives control from a processor s instruction that directly and indirectly indexed causes the selected first value, second value or address value to be applied to the memory as a source or destination address for memory load and stores.